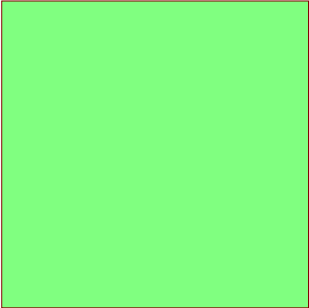
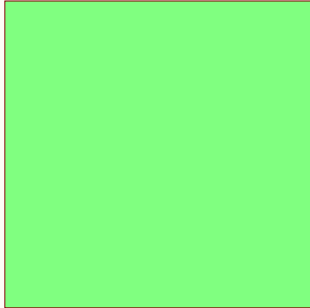


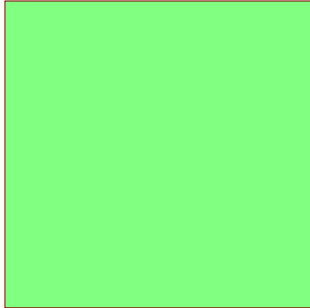
Designator
[01] - COVER PAGE.SchDoc



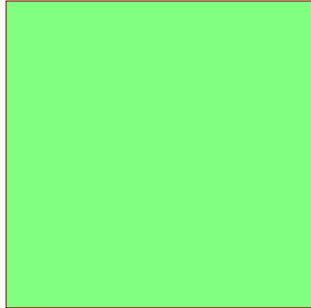
Designator
[02] - BLOCK DIAGRAM.SchDoc



Designator
[03] - CONNECTORS.SchDoc



Designator
[04] - DOC REVISION HISTORY.SchDoc



TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Project and Version

Mark Not Fitted Components as

NF

Net Class Example



Differential signal example



TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

Title 17B24		Kronotech Srl <i>Via Adriatica, 284</i> <i>33030 - Basaldella (UD)</i> <i>Italy</i>
Size: A3	Revision: V0	
Date: 07/01/2025	Sheet 1 of 5	

17B24

Variant: [01] - Sample Production

07/01/2025
V0

RELEASED

Page	Index	Page	Index	Page	Index	Page	Index
1	COVER PAGE	11		21		31	
2	BLOCK DIAGRAM	12		22		32	
3	CONNECTORS	13		23		33	
4	DOC REVISION HISTORY	14		24		34	
5		15		25		35	
6		16		26		36	
7		17		27		37	
8		18		28		38	
9		19		29		39	
10		20		30		40	

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational
design notes .

DESIGN NOTE:
Example text for critical
design notes.

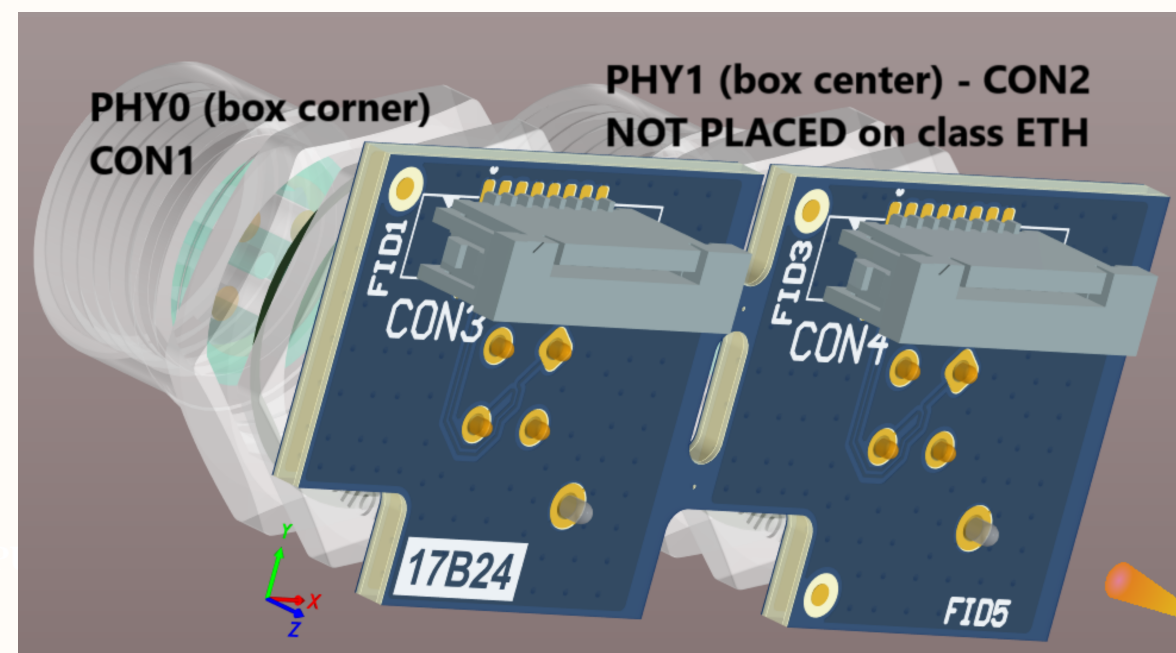
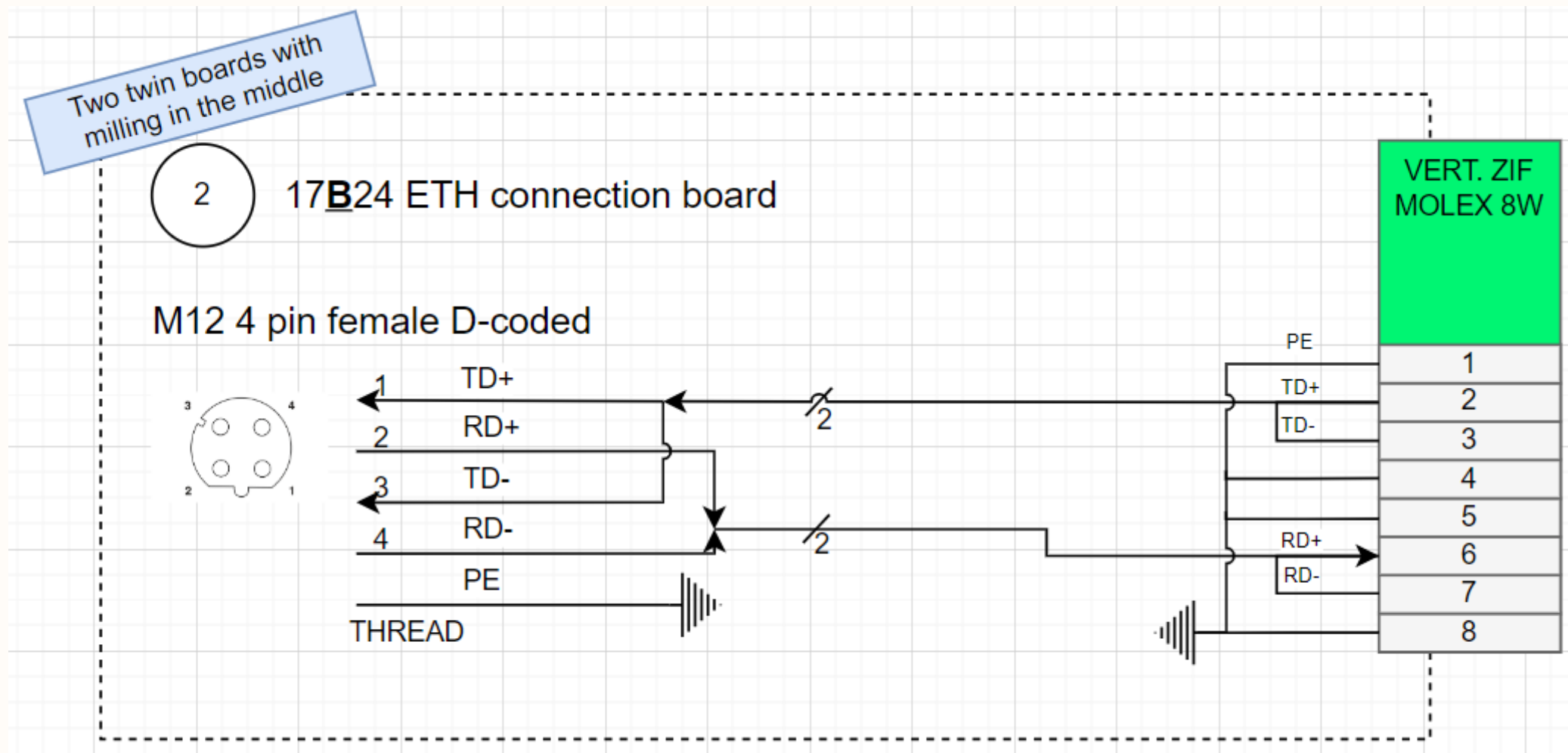
DESIGN NOTE:
Example text for cautionary
design notes.

LAYOUT NOTE:
Example text for critical
layout guidelines.

17B24

(Block Diagram)

PCB containing 2 sets and a fiducial in the middle to be broken (PHY1 not placed in case of classical ETH)
OR
PCB containing a single set (2x needed for PROFINET and such).

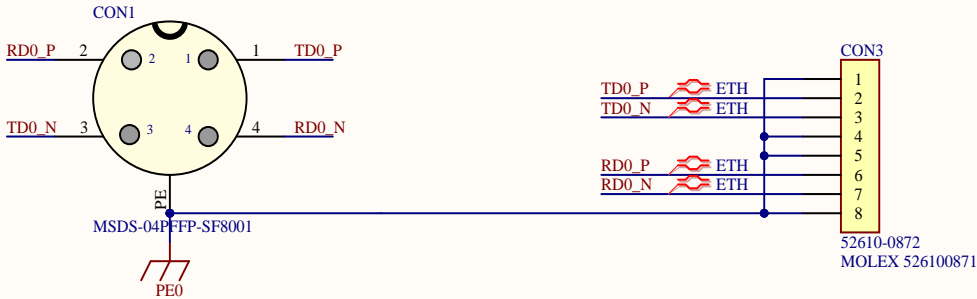


Ethernet connection pin assignment:
1 x M12, D-coded, 4 pin, female

Pin	Description
1	TD+
2	RD+
3	TD-
4	RD-
Thread	PE

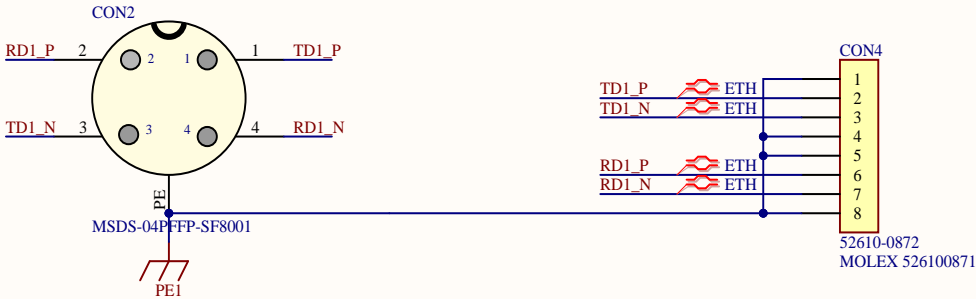
CONNECTORS

ZIF 8W ETH PHY0 to main board



Opposite side of power connector

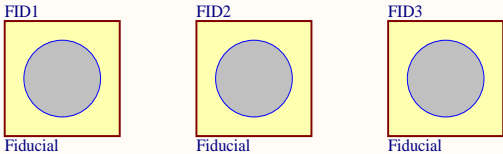
ZIF 8W ETH PHY1 to main board



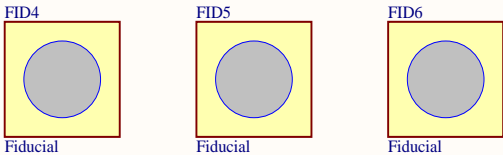
NOT PRESENT on CLASSICAL ETH

FIDUCIALS

TOP

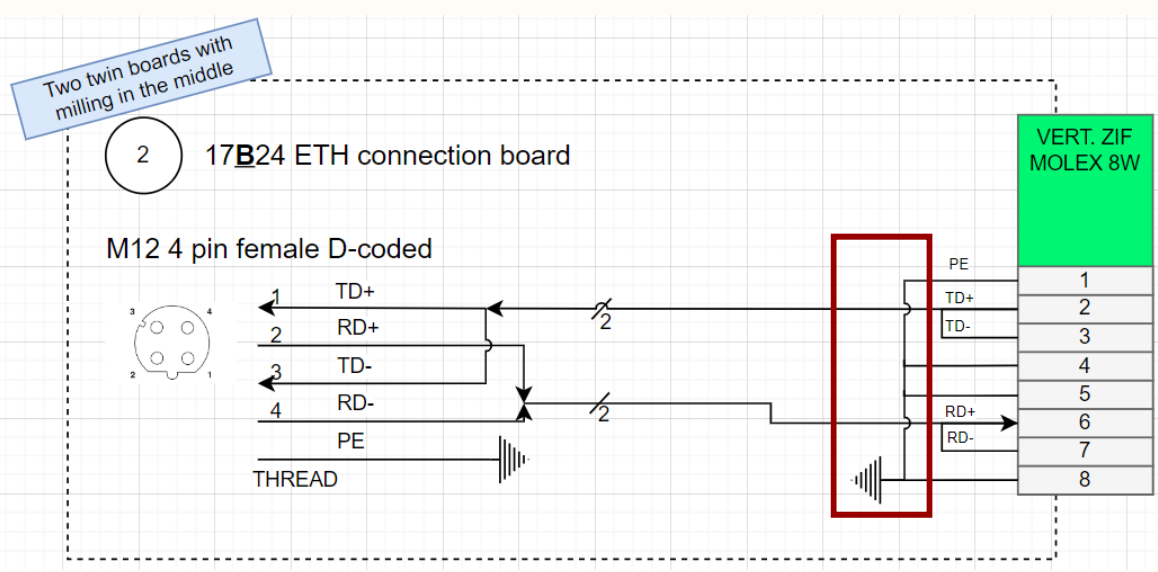
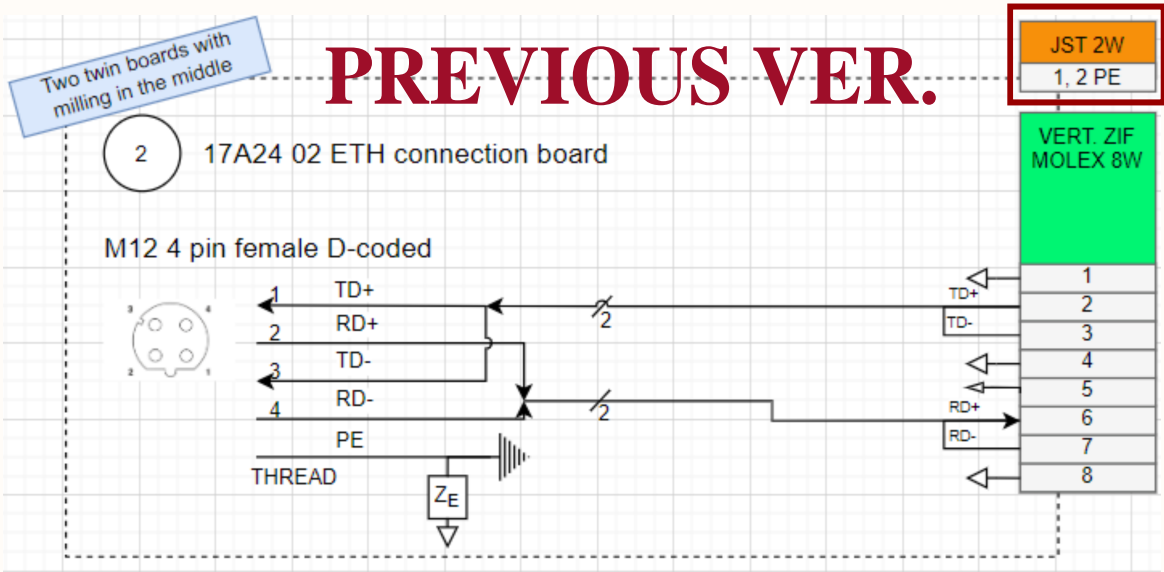


BOT



DOC: REVISION HISTORY

17A24 > 17B24: GND replaced with PE on ZIF connector.
JST connectors removed (were bringing PE to 14A24) - (CON5, CON6).
ZE (R-C networks) between PE and GND removed (W1, W2, R1, R2, C1, C2).



CLOCKS (CPU & PCIe)